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| **RAJESH S** | PHOTO |
| Office of Career Advancement and Networking, Alliance University, Chandapura-Anekal Main Road, Bengaluru, 562106  Mob: +91-8217454465  Linkedin ID: https://www.linkedin.com/in/contactrajeshs/  Email ID: <srajeshBTECH21@ced.alliance.edu.in> |

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| **CAREER OBJECTIVE** |

I aspire to integrate my academic expertise in VLSI with practical experience in a prominent Electronics company, advancing engineering skills and interpersonal abilities through active project contribution.

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| **PROFILE SUMMARY** |

Enthusiastic Electronics and communication engineering student with a passion for VLSI, with a desire to acquire new skills and a strong desire to put those abilities to use someplace. A fresher with aptitude for technical proficiency, collaborative teamwork, leadership skills and effective communication. Familiar with tools such as MATLAB, Arduino IDE, Vivado, CISCO packet tracer.

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| **ACADEMICS** |

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| **Duration** | **Qualification** | **GPA** | **Percentage** |
| 2021-25 | B.Tech in Electronics and Communication Engineering from Alliance University, Bangalore( up to 5th sem) | **7.54/10** | **75.42%** |
| 2020-21 | Class 12 from Bellary Independent PU College, Bellary | **8.31/10** | **83.1%** |
| 2018-19 | Class 10 from Best Residential School and  college Bellary,Bellary | **7.96/10** | **79.68%** |

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| **Value Added Certificates** | |
| **Google** | |
| **The Bits and Bytes of Computer Networking** | * Computer Networking * Network Architecture * Network Model * Critical Thinking |
| **University Of Colorado Boulder** | |
| **Hardware descriptive language for**  **FPGA Design** | * Designing FPGA logic * Writing Code in Verilog * Designing Test branches * Simulating FPGA designs |
| **VLSI Design**  **And**  **Verification** | * Basics of system Verilog * Understanding Different Circuits Through Verilog * VLSI Design logic |
| **TESSOLVE SEMICONDUCTOR PVT LTD - October 9, 2023** | |
| **Semiconductor Industry Training - VLSI Design & Verification** | * Introduction to Hardware Description Language VHDL * Understand Sequential Circuits * Concept of FSM, Mealy and Moore Machine * Writing Code in Verilog and System Verilog |

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| PUBLICATIONS |
| **Automated Macular Edema Identification and Severity Assessment Using Computer Vision**  **Image Processing Tools**  IIP Series Volume 3 2023 Chapter Status .Chapter ID “E4S9G59- 26AUPP30” |

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| PROJECTS |
| **Automatic wireless EV Charging system**  **Alliance University,2023-2024**  "Our project aims to develop an automatic wireless EV charging system. This system will use wireless charging technology to enable electric vehicles to recharge without the need for physical cables. It will offer a convenient and efficient charging solution for EV owners, promoting the adoption of electric vehicles and reducing reliance on traditional fossil fuels." |
| **Alcohol Detection and Accident Prevention System**  **Alliance University,2023**  Demonstrating proficiency in safety engineering by combing alcohol detection capabilities with the automated system intervention. |
| **IOT Based Steam Tea Dispenser**  **Alliance University,2022-23**  "Our smart steam tea maker uses innovative technology to control water temperature for the perfect steam level. It includes a steeping timer to prevent overstepping, ensuring a delightful brew every time." |
| **Chemical detector and automated home appliances shutdown**  **Alliance University,2022-23**  “Our project Enhance home safety with a smart chemical detector and automated appliance shut down for a secure living environment.” |
| **IOT Based Soil moisture Detection**  **Alliance University, 2022**  Demonstrating expertise in sensor technology to optimize irrigation strategies for improved agricultural efficiency |

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| **Skills** | |
| **Technical** | c/c++, Matlab , Arduino IDE, Microsoft Excel, Cisco Packet Tracer, Vivado |
| **Soft** | Project Management, Critical Thinking, Problem Solving, Team Leading |

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| **AWARDS & ACHIEVEMENTS** | |
| **Academic** | * Participation certificate for Working model in TECHNO FAIR – SPRING MEETING & EXHIBIT ON ADVANCES IN SCIENCE AND ENGINEERING, Alliance University, 2023 * Participation certificate for Poster Presentation in TECHNO FAIR – SPRING MEETING & EXHIBIT ON ADVANCES IN SCIENCE AND ENGINEERING, Alliance University, 2023 |
| **Extra and Co-Curricular** | * Served as a Student Coordinator for IEEE Event, Alliance University, 2023 * Actively engaged as student coordinator for Proglint’s Computer Vision National Hackathon, Alliance university, 2023 * Played an active role as a Student Coordinator, NSS club to maintain the Temple’s untaintedness |

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| INTERESTS |
| Trading, sketching, Cricket ,Football |

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| **PERSONAL DETAILS** | |
| **Permanent Address** | Hospate Road, Bellary cantonment, Vinayaka Nagar, Allipura,Bellary-583014 |
| **Date of Birth** | 14th February 2002. |
| **Languages** | English, Hindi, Kannada, Telugu. |